PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Christian Panis

Group Art Unit: Not Assigned

Serial No.:   Not Assigned

Examiner: Not Assigned

Filed: Herewith

Docket No.: 1406/39

For: DATA PROCESSING METHOD

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PRELIMINARY AMENDMENT

Honorable Commissioner for Patents
BOX PATENT APPLICATION
Washington, D.C. 20231

Dear Sir:

Kindly amend the subject application as follows:

IN THE SPECIFICATION:

Please insert the paragraph heading on page 1 of the English translation of the subject application, before line 5, as follows:

--Technical Field --.

Please insert the paragraph heading on page 1 of the English translation of the subject application, before line 10, as follows:

--Background Art --.

Please insert the paragraph heading on page 3 of the English translation of the subject application, before line 1, as follows:

--Summary of the Invention--.

Please insert the paragraph heading on page 4 of the English translation of the subject application, before line 23, as follows:

--Brief Description of the Drawings--.

Please insert the paragraph heading on page 5 of the English translation of the subject application, before line 9, as follows:

--Detailed Description of the Invention--.

<u>IN THE CLAIMS:</u>

Please delete the paragraph heading on page 8 of the English translation of the subject application, line 1, and insert in place thereof the paragraph heading as follows:

<center>--<u>CLAIMS</u>--</center>

Please insert the paragraph heading on page 8 of the English translation of the subject application, before claim 1, the following:

-- <u>What is claimed is:</u> --.

Please amend claims 1-7 as follows:

1.   (Amended) A data processing method using a multiplicity of processors which operate in parallel and to which a respective command for data processing is supplied simultaneously, at least one of the processors being alternatively supplied with a program flow control command or a condition command, the supplying of the condition command deactivating the parallel execution of a further command in at least one of the further processors.

2.   (Amended) The data processing method as claimed in claim 1, wherein the supplying of the condition command has the effect that the computational result of one of the processors is not written back into a target register which is provided.

3.   (Amended) The data processing method as claimed in claim 1, wherein the supplying of the condition command has the effect that an address is not calculated.

4.   (Amended) The data processing method as claimed in claim 1, wherein the supplying of the condition command has the effect that a command is not executed by the at least one of the further processors.

5.   (Amended) The data processing method as claimed in claim 1, wherein the further commands comprise arithmetic computational commands and/or move commands.

6.   (Amended) The data processing method as claimed in claim 1, wherein the condition which is associated with the condition command is the same for all of the further processors.

7.   (Amended) The data processing method as claimed in claim 1, wherein the condition which is associated with the condition command is different from all the further processors.

<center><u>REMARKS</u></center>

The amendments to the specification as set forth above are intended to clarify and set apart the various sections of the subject application.

The amendments to the claims as set forth above are intended to remove all multiple dependent claims from the subject application and to more particularly point out and distinctly claim the subject invention.

Attached hereto is a marked-up version of the specification and claims 1-7, which illustrates all of the changes made to the specification and claims pursuant to

37 CFR §1.121. The attached page is captioned "**Version With Markings To Show Changes Made**". Deleted language is bracketed and added language is underlined.

The Commissioner is hereby authorized to charge any deficiencies or credit any overpayments in connection with the filing of this correspondence to Deposit Account No. **50-0426**.

Respectfully submitted,

JENKINS & WILSON, P.A.

Date: 1-16-02   By: _Richard E. Jenkins_

Richard E. Jenkins
Reg. No.: 28,428

Suite 1400 University Tower
3100 Tower Boulevard
Durham, North Carolina 27707
Telephone: (919) 493-8000
Facsimile: (919) 419-0383

1406/39   REJ/lsg

Version With Markings To Show Changes Made

IN THE SPECIFICATION:

The paragraph heading has been inserted on page 1 of the English translation of the subject application, before line 5, as follows:

Technical Field

The paragraph heading has been inserted on page 1 of the English translation of the subject application, before line 10, as follows:

Background Art

The paragraph heading has been inserted on page 3 of the English translation of the subject application, before line 1, as follows:

Summary of the Invention

The paragraph heading has been inserted on page 4 of the English translation of the subject application, before line 23, as follows:

Brief Description of the Drawings

The paragraph heading has been inserted on page 5 of the English translation of the subject application, before line 9, as follows:

Detailed Description of the Invention

IN THE CLAIMS:

The paragraph heading "Patent Claims" on page 8 of the English translation of the subject application has been deleted and the paragraph heading has been inserted in place thereof as follows:

CLAIMS

The paragraph heading has been inserted on page 8 of the English translation of the subject application, before claim 1, as follows:

What is claimed is:

1.   (Amended) A data processing method using a multiplicity of processors [(P1 – P5)] which operate in parallel and to which a respective command [(CMP1, CMP2, MOV1, MOV2, FSEL)] for data processing is supplied simultaneously, at least one of the processors [(P5)] being alternatively supplied with a program flow control command or a condition command [(FSEL)], the supplying of the condition command [(FSEL)] deactivating the parallel execution of a further command [(CMP1, CMP2, MOV1, MOV2)] in at least one of the further processors [(P1 – P4)].

2.   (Amended) The data processing method as claimed in claim 1, wherein the supplying of the condition command [(FSEL)] has the effect that the computational result of one of the processors [(P1, P2)] is not written back into a target register [(RF)] which is provided.

3.   (Amended) The data processing method as claimed in claim 1 [or 2], wherein the supplying of the condition command [(FSEL)] has the effect that an address is not calculated.

4.   (Amended) The data processing method as claimed in claim 1, [2 or 3,] wherein the supplying of the condition command [(FSEL)] has the effect that a command is not executed by the at least one of the further processors [(P1 – P4)].

5.   (Amended) The data processing method as claimed in [one of the preceding claims] claim 1, wherein the further commands [(CMP1, CMP2, MOV1, MOV2)] comprise arithmetic computational commands and/or move commands.

6.   (Amended) The data processing method as claimed in [one of the preceding claims] claim 1, wherein the condition which is associated with the condition command [(FSEL)] is the same for all of the further processors [(P1 – P4)].

7.   (Amended) The data processing method as claimed in [one of the preceding claims] claim 1, wherein the condition which is associated with the condition command [(FSEL)] is different from all the further processors [(P1 – P4)].